UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,285	12/23/2003	Stephan J. Jourdan	2207/17416	7862

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EXAMINER
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ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/743,285	JOURDAN ET AL.
	Examiner	**Art Unit**	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>23 January 2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-27</u> is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-5,11,17-19 and 25-27</u> is/are rejected.

7)☒ Claim(s) <u>6-10,12-16 and 20-24</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>23 December 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☐ All   b)☐ Some * c)☐ None of:

       1.☐ Certified copies of the priority documents have been received.

       2.☐ Certified copies of the priority documents have been received in Application No. _____.

       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-27 as presented on 12/23/2003 are pending in the instant application.

Of these, there are 4 independent claims and 23 dependent claims.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.   **Claims 1-5, 11, 17-19, and 25-27** are rejected under 35 U.S.C. 102(b) as being

anticipated by Doing et al. (US 6,161,166).

1.   **Claim 1** is taught by Doing as:

a.   *A method of processing addresses, comprising: receiving a full linear*

address of an instruction, and reducing a size of the full linear address to obtain a

reduced linear address. Column 10 lines 26-36 show that a hash function is

used to convert the effective address to a 7 bit value.

2.   **Claim 2** is taught by Doing as:

b.   *The method of claim 1, further including hashing a subset of the full linear*

address to reduce the size of the full linear address.   Column 10 lines 26-27

show that bits 45-51 of the effective address are used in the hash function.

3.   **Claim 3** is taught by Doing as:

c.   *The method of claim 2, wherein the full linear address includes one or*

more line offset bits and one or more set index bits, the method further including

isolating the offset bits and the set index bits from the hashing. Column 10 lines

26-27 show that only bits 45-51 of the effective address are used in the hash

function, therefore isolating the offset and set index bits from the hashing.

4.   **Claim 4** is taught by Doing as:

d.   *The method of claim 2, further including hashing a thread signature with*

the subset of the full linear address. The hash function shown in column 10 lines

34-35 includes the input ActT, which is shown in column 10 lines 31-32 to

indicate which of the threads is active.

5.   **Claim 5** is taught by Doing as:

e.   *The method of claim 1, further including retrieving a data block from a data*

array if the reduced linear address corresponds to a tag in a tag array, the tag

array being associated with the data array. Column 10 lines 20-24 show that the

ERAT contains a portion of the effective address, the tag, and a portion of a real

address, a data block.

6.   **Claim 11** is taught by Doing as:

f.   *A method of retrieving data, comprising: receiving a full linear address of*

an instruction; reducing a size of the full linear address to obtain a reduced linear

address. Column 10 lines 26-36 show that a hash function is used to convert the

effective address to a 7 bit value.

g.   *The reducing including hashing a subset of the full linear address.*

Column 10 lines 26-27 show that bits 45-51 of the effective address are used in

the hash function.

h.   *Isolating one or more cache line offset bits of the full linear address and*

one or more set index bits of the full linear address from the hashing. Column 10

lines 26-27 show that only bits 45-51 of the effective address are used in the

hash function, therefore isolating the offset and set index bits from the hashing.

i.   *And retrieving a data block from a data array if the reduced linear address*

corresponds to a tag in a tag array, the tag array being associated with the data

array. Column 10 lines 20-24 show that the ERAT contains a portion of the

effective address, the tag, and a portion of a real address, a data block.

7.   **Claim 17** is taught by Doing as:

j.   *An address processing unit comprising: a data structure having a data array and a tag array.* See figure 4A, which shows ERAT, item 301, containing a section for the effective address, the tag array, and a section for the real address, the data array.

k.   *A reduction module to reduce a size of a full linear address of an instruction to obtain a reduced linear address.* Column 10 lines 26-36 show that a hash function is used to convert the effective address to a 7 bit value.

l.   *And a retrieval module to retrieve a data block from the data array if the reduced linear address corresponds to a tag in the tag array.* Column 10 lines 36-39 show that the appropriate ERAT entry is selected by select logic 401 of figure 4A in accordance with the hash function.

8.   **Claim 18** is taught by Doing as:

m.   *The address processing unit of claim 17, wherein the reduction module is to hash a subset of the full linear address to reduce the size of the full linear address.* Column 10 lines 26-27 show that bits 45-51 of the effective address are used in the hash function.

9.   **Claim 19** is taught by Doing as:

n.   *The address processing unit of claim 18, wherein the full linear address is to include one or more line offset bits and one or more set index bits, the reduction module to isolate the offset bits and the set index bits from the hashing.*

Column 10 lines 26-27 show that only bits 45-51 of the effective address are

used in the hash function, therefore isolating the offset and set index bits from

the hashing.

10.   **Claim 25** is taught by Doing as:

o.   *A computer system comprising: a random access memory.* Figure 1A

item 102.

p.   *A bus coupled to the memory.* Figure 1A item 109

q.   *And a processor coupled to the bus, the processor to receive an*

instruction from the memory and including an address processing unit having a

data structure, a reduction module and a retrieval module. Figure 1A item 101.

CPU 101 is shown to contain I-cache 106. I-cache 106 is shown in column 8

lines 3-4 to contain ERAT 301. ERAT 301 contains a data structure, a reduction

module, and a retrieval module.

r.   *The data structure having a data array and a tag array.* Figure 4A shows

ERAT 301, which contains a section for the effective address, the tag array, and

a section for the real address, the data array.

s.   *The reduction module to reduce a size of a full linear address of the*

instruction to obtain a reduced linear address. Column 10 lines 26-36 show that

a hash function is used to convert the effective address to a 7 bit value.

t.   *The retrieval module to retrieve a data block from the data array if the*

reduced linear address corresponds to a tag in the tag array. Column 10 lines

36-39 show that the appropriate ERAT entry is selected by select logic 401 of

figure 4A in accordance with the hash function.

11.   **Claim 26** is taught by Doing as:

u.   *The computer system of claim 25, wherein the reduction module is to hash*

a subset of the full linear address to reduce the size of the full linear address.

Column 10 lines 26-27 show that bits 45-51 of the effective address are used in

the hash function.

12.   **Claim 27** is taught by Doing as:

v.   *The computer system of claim 26, wherein the full linear address is to*

include one or more line offset bits and one or more set index bits, the reduction

module to isolate the offset bits and the set index bits from the hashing. Column

10 lines 26-27 show that only bits 45-51 of the effective address are used in the

hash function, therefore isolating the offset and set index bits from the hashing.

Allowable Subject Matter

13.   **Claims 6-10, 12-17, and 20-24** are objected to as being dependent upon a

rejected base claim, but would be allowable if rewritten in independent form including all

of the limitations of the base claim and any intervening claims.

14.   **Claims 6, 12, and 20** recite the limitation "wherein the data array is a prediction

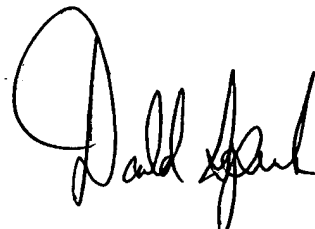array of a branch predictor, the data block including a branch prediction address having

a size that equals a size of the reduced linear address." The invention disclosed by

Doing does not teach or suggest using a reduced liner address to locate a branch

prediction address.

15.   **Claims 7, 13, and 21** recite the limitation "wherein the data array is a cache

array of a cache, the data block including a stored linear address having a size that

equals the size of the full linear address." While the invention disclosed by Doing is a

cache, it only stores bits 0-46 of the effective address. Column 10 lines 42-46 state that

is unnecessary to hold bits 47-51 because they were used in the hash function.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-

5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

DONALD SPARKS
SUPERVISORY PATENT EXAMINER

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Business Center (EBC) at 866-217-9197 (toll-free).

Jared I Rutz
Examiner
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